AMENDMENTS TO THE CLAIMS:

1. (Previously Presented) A charge pump circuit comprising:

a plurality of switching transistors connected in series between an output terminal and reference potential terminal of the charge pump circuit, wherein the plurality of switching transistors includes a first transistor connected to the reference potential terminal and a second transistor connected to the first transistor, and wherein the first transistor has a control terminal provided with a first clock signal, and the second transistor has a control terminal provided with a second clock signal, the first and second clock signals having inverted phases;

a capacitor connected to a node between the first and second transistors and having a first terminal and a second terminal; and

a delay circuit connected between the second terminal of the capacitor and the control terminal of the first transistor, wherein the delay circuit delays the first clock signal, which is provided to the control terminal of the first transistor, by a predetermined time and provides the delayed first clock signal to the second terminal of the capacitor.

2. (Original) The charge pump circuit according to claim 1, further comprising:

a buffer circuit functioning between a predetermined power supply potential and a potential at the node for receiving the first clock signal and providing a buffered clock signal to the delay circuit and the control terminal of the first transistor.

3. (Original) The charge pump circuit according to claim 2, further comprising:

a timing adjustment circuit connected to the buffer circuit to generate the first and second clock signals so that a period during which the first and second transistors are simultaneously deactivated exists.

4. (Original) The charge pump circuit according to claim 3, wherein the timing adjustment circuit includes:

a first inverter for receiving the delayed first clock signal, inverting the first clock signal, and generating an inverted first clock signal;

a second inverter for inverting an original clock signal provided to the charge pump circuit and generating an inverted original clock signal;

a first NAND circuit connected to the first and second inverters for receiving the inverted original clock signal and the inverted first clock signal to generate the second clock signal;

a third inverter for receiving the second clock signal and generating an inverted second clock signal; and

a second NAND circuit connected to the third inverter for receiving the original clock signal and the inverted second clock signal to generate the first clock signal.

5. (Original) The charge pump circuit according to claim 3, wherein the timing adjustment circuit includes:

a first NOR circuit for receiving an original clock signal provided to the charge pump circuit and the second clock signal to generate a first NOR logic signal;

a first inverter connected to the first NOR circuit for inverting the first NOR logic signal and generating the first clock signal;

a second inverter for inverting the original clock signal and generating an inverted original clock signal;

a second NOR circuit connected to the second inverter for receiving the first clock signal and the inverted original clock signal to generate a second NOR logic signal; and

a third inverter connected to the second NOR circuit for inverting the second NOR logic signal and generating the second clock signal.

6. (Original) The charge pump circuit according to claim 3, wherein the delay circuit temporarily sets the second terminal of the capacitor in a high impedance state and, after delaying the first clock signal by the predetermined time from when the first clock signal is inverted, provides the delayed first clock signal to the second terminal of the capacitor.

7. (Original) The charge pump circuit according to claim 6, wherein the delay circuit includes:

third and fourth transistors connected in series between a high potential power supply and a low potential power supply, wherein a second node between the third and fourth transistors is connected to the second terminal of the capacitor;

a first logic circuit for providing a first control signal to a control terminal of the third transistor; and

a second logic circuit for providing a second control signal to a control terminal of the fourth transistor, wherein one of the first and second logic circuits generates its control signal base on the first clock signal and the control signal of the other one of the first second logic circuits so that a period during which the third and fourth transistors are simultaneously deactivated exists.

8. (Original) The charge pump circuit according to claim 7, wherein the third transistor is a p-channel transistor connected between the high potential power supply and the second terminal of the capacitor, and the fourth transistor is an n-channel transistor connected between the low potential power supply and the second terminal of the capacitor, the first logic circuit being a NOR circuit, and the second logic circuit being an AND circuit, wherein the NOR circuit performs a NOR logic operation based on the first clock signal and the second control signal to generate a NOR logic signal, and the AND circuit performs a logic AND operation based on the first clock signal and the first control signal to generate the second control signal,

and wherein the delay circuit further includes an inverter connected to the NOR circuit to invert the NOR logic signal and generate the first control signal.

9. (Original) The charge pump circuit according to claim 2, wherein the delay circuit temporarily sets the second terminal of the capacitor in a high impedance state and, after delaying the first clock signal by predetermined time from when the first clock signal is inverted, provides the delayed first clock signal to the second terminal of the capacitor.

10. (Original) The charge pump circuit according to claim 9, wherein the delay circuit includes:

third and fourth transistors connected in series between a high potential power supply and a low potential power supply, wherein a second node between the third and fourth transistors is connected to the second terminal of the capacitor;

a first logic circuit for providing a first control signal to a control terminal of the third transistor; and

a second logic circuit for providing a second control signal to a control terminal of the fourth transistor, wherein one of the first and second logic circuits generates its control signal based on the first clock signal and the control signal of the other one of the first and second logic circuits so that a period during which the third and fourth transistors are simultaneously deactivated exists.

11. (Original) The charge pump circuit according to claim 10, wherein the third transistor is a p-channel transistor connected between a high potential power supply and the second terminal of the capacitor, and the fourth transistor is an n-channel transistor connected between the low potential power supply and the second terminal of the capacitor, the first logic circuit being a NOR circuit, and the second logic circuit being an AND Circuit, wherein the NOR circuit performs a NOR logic operation based on the first clock signal and the second control signal to generate a NOR logic signal, and the AND circuit performs a logic AND operation based on the first clock signal and the first control signal to generate the second control signal, and wherein the delay circuit further includes an inverter connected to the NOR circuit to invert the NOR logic signal and generate the first control signal.